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PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Add a second PCIe lane to Type 1216 SDIO Based LGA Module
DATE:	May 23, 2017
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.1
SPONSOR:	Jim Panian, Qualcomm Technologies Inc.

Part I

1. Summary of the Functional Changes

The M.2 Type 1216 Land Grid Array (LGA) Connectivity module is modified to add a second PCIe lane. Referring to Figure 99 on page 127:

Pad #	Current	New
21	Reserved	PETn1
22	Reserved	PETp1
24	Reserved	PERn1
25	Reserved	PERp1

2. Benefits as a Result of the Changes

Connectivity applications that require two PCIe lanes may be implemented as either a 1216 LGA module or as an Add-in Card.

3. Assessment of the Impact

The additional PCIe lane uses pins that were previously marked as Reserved.

4. Analysis of the Hardware Implications

Hardware changes are required to take advantage of this new optional capability.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

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Part II

Detailed Description of the changes

Change Table 15, page 102, as follows:

PCIe ~~(up to two instances)~~	PERp0, PERn0/ PETp0, PETn0/ PERp1, PERn1/ PETp1, PETn1/	I/O	PCIe TX/RX Differential signals defined by the *PCI Express ~~Card Electromechanical (CEM)~~ CEM Specification*.

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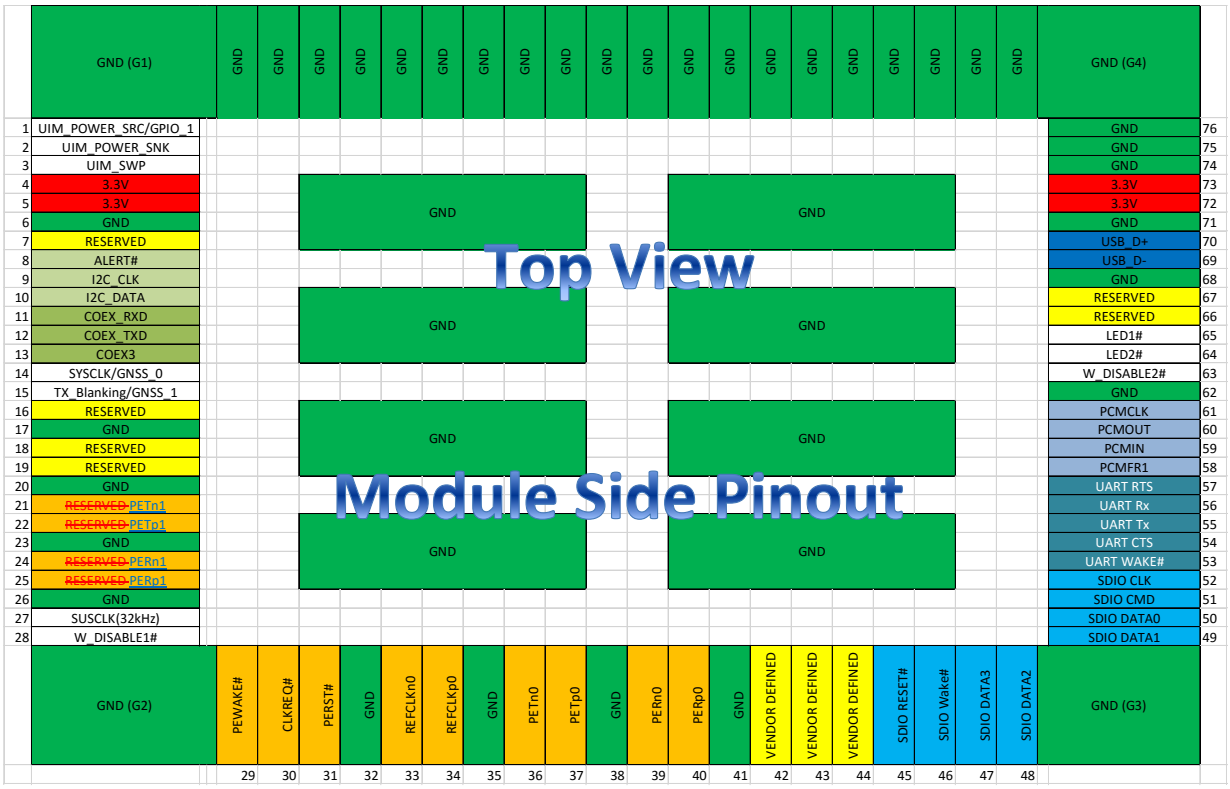
Change Figure 99, page 127, as follows:



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Change Figure 109, page 188, as follows: